

WHAT IS CLAIMED IS:

1 1. A programmable logic device (PLD) comprising:
2 input/output (I/O) interface having a first plurality of I/O register blocks,
3 the first plurality of I/O register blocks being partitioned into a second plurality of I/O
4 sections each I/O section having N data I/O register blocks and a strobe circuit,
5 wherein each of the N data I/O register blocks is configured to store multiple bits of
6 data, and each strobe circuit is configured to generate a local strobe signal that drives a
7 local clock line coupling to clock inputs of the N data I/O register blocks, the N data
8 I/O register blocks and the strobe circuit in each I/O section being coupled to a
9 corresponding number of device pins; and
10 programmable logic circuitry coupled to the I/O interface.

1 2. The PLD of claim 1 wherein the strobe circuit in each I/O section
2 is configured to shift a phase of an input strobe signal received at a respective strobe
3 pin.

1 3. The PLD of claim 2 further comprising a master phase control
2 circuit coupled to receive a master clock signal and configured to generate a phase
3 control signal that controls a phase delay in the strobe circuit in one or more of the
4 second plurality of I/O sections.

1 4. The PLD of claim 3 wherein the second plurality of I/O sections
2 are grouped into a third plurality of I/O banks.

1 5. The PLD of claim 4 wherein a separate master phase control
2 circuit is provided for I/O sections in each of the third plurality of I/O banks.

1 6. The PLD of claim 1 wherein each I/O register block comprises
2 two registers, one of which stores a first incoming bit of data at a rising edge of the
3 local strobe signal and the other stores a second incoming bit of data at a falling edge
4 of the local strobe signal.

1 7. The PLD of claim 6 wherein the strobe circuit in each I/O section
2 comprises a programmable phase delay circuit that is configured to shift a phase of the
3 local strobe signal such that an edge of the local strobe signal occurs substantially at
4 the center of a data pulse.

1 8. The PLD of claim 7 wherein the phase delay is about 90 degrees.

1 9. The PLD of claim 1 wherein each I/O section further comprises
2 one or more general purpose register blocks coupled to respective device pins.

1 10. The PLD of claim 1 wherein, in each I/O section, the strobe
2 circuit is located as close to a center the N data I/O register blocks as possible wherein
3 an equal number of data I/O register blocks are located in either sides of the strobe
4 circuit.

1 11. The PLD of claim 1 wherein the programmable logic circuitry
2 comprises a plurality of programmable logic blocks coupled via a network of a
3 plurality of programmable vertical and horizontal interconnect lines.

1 12. A computing system comprising a multiple-data-rate memory
2 circuit coupled to a programmable logic device (PLD) as set forth in claim 1.

1 13. The computing system of claim 12 wherein the multiple-data-rate
2 memory circuit comprises a double data rate synchronous dynamic random access
3 memory.

1 14. A method of operating a programmable logic device (PLD)
2 comprising:
3 receiving N groups of data bits each group having M data signals and a
4 corresponding data strobe signal;
5 partitioning I/O register blocks inside the PLD into a corresponding N
6 I/O modules, each module having M I/O register blocks and a strobe circuit coupled to
7 receive a respective group of M data signals and data strobe signal; and
8 driving clock inputs of the M I/O register blocks in each of the N I/O
9 modules using an independent clock network that is local to each of the N I/O
10 modules.

1 15. The method of claim 14 further comprising programmably
2 shifting a phase of the data strobe signal before driving the clock inputs of the M I/O
3 register blocks.

1 16. The method of claim 15 wherein the programmably shifting of
2 the phase of the data strobe comprises generating phase control signal in response to a
3 system clock.